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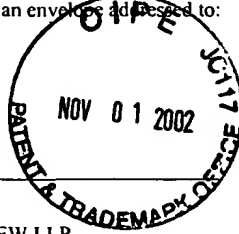
Assistant Commissioner for Patents
Washington, D.C. 20231

On 10.29.02

TOWNSEND and TOWNSEND and CREW LLP

By: Edward Masinas
Edward Masinas

PATENT
Attorney Docket No.: 015114-053500US
Client Reference No.: A618



IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

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In re application of:

ANDREW CROSLAND et al.

Application No.: 09/880,734

Filed: June 12, 2001

For: EMBEDDED PROCESSOR WITH
WATCHDOG TIMER FOR
PROGRAMMABLE LOGIC

Examiner: To Be Assigned

Art Unit: 2819

SUPPLEMENTAL INFORMATION
DISCLOSURE STATEMENT UNDER 37
CFR §1.97 and §1.98

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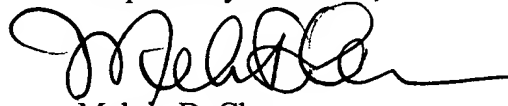
The references cited on attached form PTO/SB/08A and PTO/SB/08B are being called to the attention of the Examiner. Copies of the references are enclosed. It is respectfully requested that the cited references be expressly considered during the prosecution of this application, and the references be made of record therein and appear among the "references cited" on any patent to issue therefrom.

As provided for by 37 CFR 1.97(g) and (h), no inference should be made that the information and references cited are prior art merely because they are in this statement and no representation is being made that a search has been conducted or that this statement encompasses all the possible relevant information.

Applicant believes that no fee is required for submission of this statement.

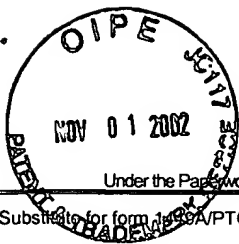
However, if a fee is required, the Commissioner is authorized to deduct such fee from the undersigned's Deposit Account No. 20-1430. Please deduct any additional fees from, or credit any overpayment to, the above-noted Deposit Account.

Respectfully submitted,



Melvin D. Chan
Reg No. 39,626

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PA 3260052 v1



PTO/SB/08A (10-01)
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Substitute for form 10/99A/PTO

INFORMATION DISCLOSURE STATEMENT BY APPLICANT

(use as many sheets as necessary)

Sheet 1 of 2

Complete if Known

Application Number	09/880,734
Filing Date	June 12, 2001
First Named Inventor	Crosland, Andrew, et. al.
Art Unit	2819
Examiner Name	To Be Assigned
Attorney Docket Number	015114-053500US

U.S. PATENT DOCUMENTS

Examiner	Cite No. ¹	Document Number	Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear
		Number Kind Code ² (if known)			
	0001	US-4,488,259	12-11-1984	Mercy	
	0002	US-4,617,479	10-14-1986	Hartmann et al.	
	0003	US-4,710,927	12-01-1987	Miller	
	0004	US-4,871,930	10-03-1989	Wong et al.	
	0005	US-5,241,224	08-31-1993	Pedersen et al.	
	0006	US-5,258,668	11-02-1993	Cliff et al.	
	0007	US-5,260,610	11-09-1993	Pedersen et al.	
	0008	US-5,260,611	11-09-1993	Cliff et al.	
	0009	US-5,412,260	05-02-1995	Tsui et al.	
	0010	US-5,436,575	07-25-1995	Pedersen et al.	
	0011	US-5,550,782	08-27-1996	Cliff et al.	
	0012	US-5,790,479	08-04-1998	Conn	
	0013	US-6,097,211	08-01-2000	Couts-Martin et al.	
	0014	US-6,233,205	05-15-2001	Wells et al.	

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FOREIGN PATENT DOCUMENTS

Examiner Initials*	Cite No. ¹	Foreign Patent Document			Publication Date MM-DD-YYYY	Name of Patentee or Applicant of Cited Document	Pages, Columns, Lines, Where Relevant Passages or Relevant Figures Appear	T ⁶
		Country Code ³	Number ⁴	Kind Code ⁵ (if known)				
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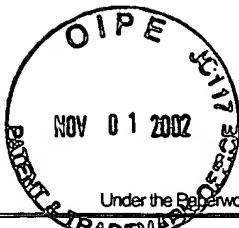
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**INFORMATION DISCLOSURE
STATEMENT BY APPLICANT**

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Sheet 2 of 2**Complete if Known**

Application Number	09/880,734
Filing Date	June 12, 2001
First Named Inventor	Crosland, Andrew, et. al.
Art Unit	2819
Examiner Name	To Be Assigned
Attorney Docket Number	015114-053500US

OTHER PRIOR ART -- NON PATENT LITERATURE DOCUMENTS

Examiner Initials *	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T ²
	0015	AITKEN, R.C., and AGARWAL, V.K., "A Diagnosis Method Using Pseudo-Random Vectors Without Intermediate Signatures," Proc. of Int. Conf. on Computer-Aided Design (ICCAD), IEEE pp. 574-577 (1989).	
	0016	Altera "APEX 20K Programmable Logic Device Family Data Sheet," May 1999, 7 pages total.	
	0017	Altera "FLEX 10K Embedded Programmable Logic Family Data Sheet," May 1999, 7 pages total.	
	0018	Altera "FLEX 8000 Programmable Logic Device Family Data Sheet," May 1999, 5 pages total.	
	0019	Altera "IEEE 1149.1 (JTAG) Boundary-Scan Testing in Altera Devices," August 1999, Application Note 39, 29 pages total.	
	0020	Altera "MAX 7000 Programmable Logic Device Family Data Sheet," May 1999, 6 pages total.	
	0021	GHOSH-DASTIDAR, J., and TOUBA, N.A., "A Rapid and Scalable Diagnosis Scheme for BIST Environments With a Large Number of Scan Chains," Proc. of IEEE VLSI Test Symposium, pp. 79-85 (2000).	
	0022	GHOSH-DASTIDAR, J., DAS, D., and TOUBA, N.A., "Fault Diagnosis in Scan-Based BIST using Both Time and Space Information," Proc. of International Test. Conf., IEEE, pp. 95-102 (1999).	
	0023	MC ANNEY, M.G. and SAVIR, J., "There is Information in Faulty Signatures," Proc. of International Test Conf., IEEE, pp. 630-636 (1987).	

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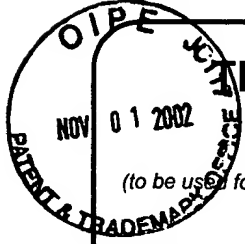
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TRANSMITTAL FORM (to be used for all correspondence after initial filing)	Application Number	09/880,734	
	Filing Date	June 12, 2001	
	First Named Inventor	Crosland, Andrew	
	Group Art Unit	2819	
	Examiner Name	To Be Assigned	
Total Number of Pages in This Submission	6	Attorney Docket Number	015114-053500US

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Firm and Individual name	Townsend and Townsend and Crew LLP Melvin D. Chan Reg. No. 39,626
Signature	
Date	October 29, 2002

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Typed or printed name	Edward Masinas
Signature	
Date	October 29, 2002

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